CLAIMS

What is claimed is:

1. A system comprising a clock doubler circuit, the clock doubler circuit comprising:

an input clock terminal;

an output clock terminal;

a first counter circuit having a clock terminal coupled to the input clock terminal and a plurality of output terminals;

a register having a plurality of data input terminals coupled to the output terminals of the first counter circuit, a clock terminal coupled to the input clock terminal, and a plurality of output terminals;

a set counter circuit having a clock terminal coupled to the input clock terminal, a plurality of data input terminals coupled to a first subset of the output terminals of the register, and an output terminal;

a reset counter circuit having a clock terminal coupled to the output clock terminal of the set counter circuit, a plurality of data input terminals coupled to a second subset of the output terminals of the register, and an output terminal; and

an output clock generator having a first input terminal coupled to the input clock terminal, a set input terminal coupled to the output terminal of the set counter circuit, a reset input terminal coupled to the output terminal of the reset counter circuit, and an output terminal coupled to the output clock terminal.

2. The system of Claim 1, wherein the first counter circuit comprises:

a first oscillator circuit having an input terminal coupled to the clock input terminal and further having an output terminal; and

a counter having an input terminal coupled to the output terminal of the first oscillator circuit and further having a plurality of output terminals coupled to the data input terminals of the register.

3. The system of Claim 2, wherein the set and reset counter circuits each comprise:

a second oscillator circuit having an input terminal coupled to the clock input terminal and further having an output terminal, the second oscillator circuit being implemented to oscillate with the same frequency as the first oscillator circuit;

a counter having an input terminal coupled to the output terminal of the oscillator circuit and further having a plurality of output terminals; and

a comparator having a first set of input terminals coupled to one of the first and second subsets of the output terminals of the register, a second set of input terminals coupled to the output terminals of the counter, and an output terminal coupled to a corresponding one of the set and reset input terminals of the output clock generator.

4. The system of Claim 1, wherein the clock doubler circuit further comprises a reset input terminal coupled to reset input terminals of the first counter circuit, the register, the set counter circuit, and the reset counter circuit.

5. The system of Claim 1, wherein the clock doubler circuit further comprises:

a reset input terminal; and

a flip-flop having a data input terminal coupled to the reset input terminal, a set terminal coupled to the data input terminal, a clock terminal coupled to the input clock terminal of the clock doubler circuit, and an output terminal coupled to reset input terminals of the first counter circuit, the register, the set counter circuit, and the reset counter circuit.

6. The system of Claim 1, wherein the first counter circuit comprises means for resetting itself after each M input clock periods, wherein M is an integer.

7. The system of Claim 6, wherein M is five.

8. The system of Claim 1, wherein the system comprises a programmable logic device (PLD), and the clock doubler circuit is implemented using programmable logic of the PLD.

9. The system of Claim 8, wherein the PLD is a field programmable gate array (FPGA).

10. The system of Claim 1, wherein the output clock generator comprises:

a logical OR circuit having a first input terminal coupled to the input clock terminal of the clock doubler circuit, a second input terminal, and an output terminal coupled to the output clock terminal of the clock doubler circuit; and

a first flip-flop having a data input terminal coupled to power high VDD, a clock terminal coupled to the output terminal of the set counter circuit, a reset terminal coupled to the output terminal of the reset counter circuit, and an output terminal coupled to the second input terminal of the logical OR circuit.

11. The system of Claim 10, wherein the output clock generator further comprises:

a second counter circuit having a clock terminal coupled to the input clock terminal, a plurality of data input terminals coupled to a third subset of the output terminals of the register, and an output terminal; and

a second flip-flop having a data input terminal coupled to the power high VDD, a clock terminal coupled to the input clock terminal, a reset terminal coupled to the output terminal of the second counter circuit, and an output terminal coupled to the first input terminal of the logical OR circuit.

12. The system of Claim 11, wherein the third subset of the output terminals of the register is the same as the second subset of the output terminals of the register.

13. A system providing from an input clock signal an output clock signal having a frequency twice that of the input clock signal, the system comprising:

first counter means for counting a first number of counts between successive first edges of the input clock signal;

means for dividing the first number to provide a divided number;

second counter means for counting a second number of counts following each first edge of the input clock signal and comparing the second number with the divided number;

first pulse generator means for providing a first pulse on the output clock signal in response to each first edge of the input clock signal; and

second pulse generator means for providing a second pulse on the output clock signal based on results of comparing the second number with the divided number.

14. The system of Claim 13, further comprising reset means for resetting the first counter means, the second counter means, the first pulse generator means, and the second pulse generator means.

15. The system of Claim 13, wherein the first counter means comprises means for resetting itself after each M input clock periods, wherein M is an integer.

16. The system of Claim 15, wherein M is five.

17. The system of Claim 13, wherein the means for dividing the first number comprises means for dividing the first number by two.

18. The system of Claim 13, wherein the second pulse generator means comprises means for providing a second pulse on the output clock signal whenever the second number is the same as the divided number.

19. The system of Claim 13, wherein the second pulse generator means comprises means for providing a second pulse on the output clock signal whenever the second number is the same as the divided number plus an offset value.

20. The system of Claim 13, wherein the second pulse generator means comprises means for providing a second pulse on the output clock signal whenever the second number is the same as the divided number minus an offset value.

21. The system of Claim 13, wherein the output clock signal has a predefined duty cycle independent of a duty cycle of the input clock signal.

22. The system of Claim 21, wherein the output clock signal has a 50 percent duty cycle.

23. The system of Claim 21, wherein the output clock signal has a 25 percent duty cycle.

24. A method of providing from an input clock signal an output clock signal having a frequency twice that of the input clock signal, the method comprising:

counting a first number of counts between successive first edges of the input clock signal;

dividing the first number to provide a divided number;

counting a second number of counts following each first edge of the input clock signal and comparing the second number with the divided number;

providing a first pulse on the output clock signal in response to each first edge of the input clock signal; and

providing a second pulse on the output clock signal based on results of comparing the second number with the divided number.

25. The method of Claim 24, wherein the counting the first number of counts and the dividing the first number to provide a divided number are repeated every M periods of the input clock signal, wherein M is an integer.

26. The method of Claim 25, wherein M is five.

27. The method of Claim 24, wherein the steps of the method are performed by a circuit implemented in a programmable logic device (PLD).

28. The method of Claim 27, wherein the PLD is a field programmable gate array (FPGA).

29. The method of Claim 24, wherein:

the first number has 2 to the power of K possible values, K being an integer;

the divided number has 2 to the power of (K-1) possible values; and

the second number has 2 to the power of (K-1) possible values.

30. The method of Claim 29, wherein K is eight.

31. The method of Claim 24, wherein the first edges are rising edges.

32. The method of Claim 24, wherein dividing the first number comprises dividing the first number by two.

33. The method of Claim 24, wherein providing a second pulse on the output clock signal based on results of comparing the second number with the divided number comprises providing a second pulse on the output clock signal whenever the second number is the same as the divided number.

34. The method of Claim 24, wherein providing a second pulse on the output clock signal based on results of comparing the second number with the divided number comprises providing a second pulse on the output clock signal whenever the second number is the same as the divided number plus an offset value.

35. The method of Claim 24, wherein providing a second pulse on the output clock signal based on results of comparing the second number with the divided number comprises providing a second pulse on the output clock signal whenever the second number is the same as the divided number minus an offset value.

36. The method of Claim 24, wherein the output clock signal has a predefined duty cycle independent of a duty cycle of the input clock signal.

37. The method of Claim 36, wherein the output clock signal has a 50 percent duty cycle.

38. The method of Claim 36, wherein the output clock signal has a 25 percent duty cycle.